

WHAT IS CLAIMED IS:

1 1. An integrated circuit comprising:
2 a control block comprising:
3 a first series of delay elements coupled to a reference clock input, each
4 delay element having an input;
5 a first selection circuit coupled to a plurality of inputs of the first series of
6 delay elements;
7 a phase detector coupled to the reference clock input and an output of the
8 selection circuit; and
9 a counter coupled to the phase detector and the series of delay elements;
10 and
11 a delay circuit coupled to the counter.

1 2. The integrated circuit of claim 1 wherein the first selection circuit
2 comprises a multiplexer.

1 3. The integrated circuit of claim 1 wherein the delay circuit comprises:
2 a second series of delay elements, each having an input; and
3 a second selection circuit coupled to a plurality of inputs of the second series of
4 delay elements.

1 4. The integrated circuit of claim 3 wherein an output of the second selection
2 circuit couples to a first storage element.

1 5. The integrated circuit of claim 4 wherein the first storage element is a flip-
2 flop.

1 6. The integrated circuit of claim 4 wherein an output of the second selection
2 circuit couples to a clock input of a first flip-flop and a complementary clock input of a second
3 flip-flop.

1 7. The integrated circuit of claim 6 wherein the first and second flip-flops are
2 coupled to a data input.

1 8. The integrated circuit of claim 3 wherein the integrated circuit is a field
2 programmable gate array.

1 9. An integrated circuit comprising:
2 a control circuit configured to receive a reference clock and provide a plurality of
3 control bits; and
4 a delay line configured to receive the plurality of stored control bits wherein the
5 delay line comprises:
6 a first series of delay elements each having an input; and
7 a first select circuit configured to a plurality of inputs of the first series of
8 delay elements.

1 10. The integrated circuit of claim 10 wherein the first select circuit is a
2 multiplexer.

1 11. The integrated circuit of claim 10 wherein the control circuit comprises:
2 a second series of delay elements configured to receive the reference clock, each
3 delay element having an input; and
4 a second select circuit coupled to a plurality of inputs of the second series of delay
5 elements.

1 12. The integrated circuit of claim 11 wherein the control circuit further
2 comprises:

3 a phase detector configured to compare the phases of the reference clock and an
4 output of second select circuit and provide an output signal; and
5 a counter configured to receive the phase detector output and provide the control
6 bits.

1 13. The integrated circuit of claim 12 wherein a polarity of the phase detector
2 output depends on the relative phase of the reference clock and the output of second select
3 circuit, and the counter is an up-down counter that counts up when the phase detector output has
4 a first polarity, and counts down when the phase detector output has a second polarity.

1 14. The integrated circuit of claim 11 wherein the first series of delay
2 elements is configured to delay a read strobe signal.

1 15. The integrated circuit of claim 15 further comprising a storage element
2 configured to receive an output of the first select circuit.

1 16. The integrated circuit of claim 10 wherein the control circuit is a delay-
2 locked loop.

1 17. The integrated circuit of claim 10 wherein the integrated circuit is a field
2 programmable gate array.

1 18. A method of delaying a data strobe signal comprising:
2 receiving a reference clock signal;
3 delaying the reference clock signal using a first number of delay elements, each
4 delay element providing a delayed reference clock signal;
5 selecting one of the delayed reference clock signals;
6 comparing the phase the reference clock signal and the selected delayed reference
7 clock signal to generate the plurality of control signals; and
8 delaying the data strobe signal using a second number of delay elements.

1 19. The method of claim 18 wherein each of the second number of delay
2 elements provide a delayed strobe signal; and the method further comprises:
3 selecting one of the delayed strobe signals.

1 20. The method of claim 19 further comprising:
2 receiving a data signal using the selected one of the delayed strobe signals.